PATENT

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Cairns et al.

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Art Unit:

Examiner:

For: DRIVING ARRANGEMENTS FOR ACTIVE MATRIX LCDs

Assistant Commissioner for Patents
Washington, D.C. 20231

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Attached please find the certified copy of the foreign application from which priority is claimed for this case:

Country: Great Britain
Application Number: 0021712.5
Filing Date: September 5, 2000

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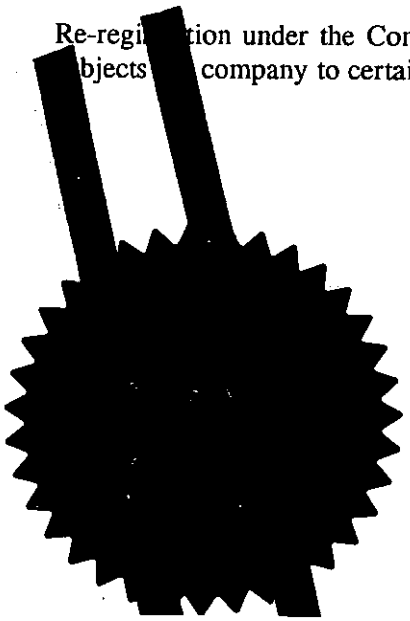

Signed J E Evans.

Dated 26 June 2001

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05SEP00 E365768-9 D01063
P01/7700 0.00-0021712.5

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Cardiff Road
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NP9 1RH

1. Your reference — JPA.P51276GB

2. Patent application number *(The Patent Office will fill in this part)* — **0021712.5**

3. Full name, address and postcode of the or of each applicant *(underline all surnames)*

   Sharp Kabushiki Kaisha
   22-22 Nagaike-cho
   Abeno-ku, Osaka 545-8522
   Japan

   Patents ADP number *(if you know it)* 66691130 01

   If the applicant is a corporate body, give the country/state of its incorporation — Japan

4. Title of the invention — Driving arrangements for active matrix LCDs

5. Name of your agent *(if you have one)*

   "Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*

   Marks & Clerk
   4220 Nash Court
   Oxford Business Park South
   Oxford OX4 2RU

   Patents ADP number *(if you know it)* 7271125001

6. If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and *(if you know it)* the or each application number

Country	Priority application number *(if you know it)*	Date of filing *(day / month / year)*

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   a) any applicant named in part 3 is not an inventor, or
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Description	9
Claim(s)	3
Abstract	1
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Priority documents	None
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Statement of inventorship and right to grant of a patent *(Patents Form 7/77)*	1
Request for preliminary examination and search *(Patents Form 9/77)*	1
Request for substantive examination *(Patents Form 10/77)*	None
Any other documents *(please specify)*	None

11. I/We request the grant of a patent on the basis of this application.

Signature Marks & Clerk Date 4/9/00
4/09/2000

12. Name and daytime telephone number of person to contact in the United Kingdom Julian Asquith (01865 397900)

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Statement of inventorship and of right to grant of a patent

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Cardiff Road
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1. Your reference JPA.P51276GB

2. Patent application number *(if you know it)* **0021712.5**

3. Full name of the or of each applicant
Sharp Kabushiki Kaisha

4. Title of the invention
Driving arrangements for active matrix LCDs

5. State how the applicant *(s)* derived the right from the inventor *(s)* to be granted a patent

By virtue of employment of the inventors by Sharp Laboratories of Europe Ltd., and by agreement with Sharp Kabushiki Kaisha.

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7. I/We believe that the person *(s)* named over the page *(and on any extra copies of this form)* is/are the inventor *(s)* of the invention which the above patent application relates to.

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Enter the full names, addresses and postcodes of the inventors in the boxes and underline the surnames

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Driving arrangements for active matrix LCDs

The invention relates to driving arrangements for active matrix liquid crystal displays (LCDs).

Figure 1 shows a typical Active Matrix Liquid Crystal Display (AMLCD) 2 comprising N rows and M columns of pixels 4. The boxes at the periphery of the matrix represent the display driver electronics, comprising a scan driver 6 with outputs connected to each row of pixel transistor gate electrodes (not shown), and a data driver with outputs connected to each column of pixel transistor source electrodes (not shown). The scan driver 6 and data driver 8 can be either analogue of digital, and can be implemented in IC technology or else monolithically using Thin Film Transistors.

In a typical AMLCD with digital drivers, an external LC controller IC supplies to the data driver a stream of digital image data, together with timing and control signals. The image data is usually clocked into an array of input registers in a line-sequential, fixed n-bit parallel RGB format, under the control of the data clock and the line (horizontal) synchronisation pulse. Once a line of n-bit RGB data has been read into the input registers, it is transferred into an array of n-bit storage registers. During the time that the subsequent line of input data is being sampled into the input registers, the data in the storage registers is input to an array of n-bit Digital-to-Analogue Converters (DACs) in order to provide analogue voltages for driving the M data lines of the active matrix. The row-sequential outputs of the scan driver determine which of the N rows of pixel transistors is activated in order to receive the data on the data lines.

In a typical AMLCD with analogue drivers, the external controller IC supplies to the data driver an analogue video signal, together with timing and control signals. There are two main types of analogue data driver, referred to as line-at-a-time or point-at-a-time. In a line at a time data driver, one line of image data is read onto storage capacitors in the driver, before being applied to the active matrix through analogue buffers. Alternatively, in a point-at-a-time analogue driver, the video data is written directly to the data lines of the active matrix, through sampling transistors which are controlled by

the timing generator of the driver.

An example of a typical LC controller IC 10 is shown in Figure 2. The controller can take input video data in either luminance and chrominance format or RGB format, and supplies either analogue or digital gamma-corrected RGB to the LC data drivers of an active matrix display. On-screen display data, for example user-interface functions such as brightness etc., is supplied by the SRAM memory 12, and used to overwrite the video data in the display mixer circuit 14 shown.

From the above description of a standard fixed-format display, it is apparent that the power consumption of the data driver, the controller IC and the display is essentially constant. Typical sources of power consumption within the data driver and IC controller include the data sampling circuits, the distributed clock and timing signals and the DAC and amplifier circuits.

Within the field of mobile communication and information products, such as internet mobile phones and Personal Digital Assistants (PDAs), there is a need for displays which are capable of showing a variety of image formats whilst at the same time minimising power consumption. An example of such an application is illustrated in Figure 3, which illustrates a conceptual mobile telephone handset capable of showing a variety of image formats, in accordance with the application that is running on the handset. Desirable image formats include high quality video data or high-resolution colour text and video overlay through to low resolution standby graphics or low frame-rate text.

Standard digital data drivers and controllers, of the type described above can meet the requirements for driving an active matrix display with video and high-resolution colour graphics, with typically 6 to 8 bits per RGB and 60Hz frame rates. However, this solution consumes unnecessary power in circumstances when the input image is of lower quality, for example with reduced colour resolution and/or frame-rate.

In order to overcome the above problem, and to support a plurality of input sources for overlay functions, the applicant has proposed a multi-format digital data driver 16 and active matrix display, as illustrated in Figure 4. In this type of data driver, the mode of operation is controlled by simple Format Control Signals (SB, MB, NB and FRC). The format is selected in order to optimise the power consumption in accordance with the type of data to be displayed. Example operating modes are: monochrome, colour of various resolution (bit-plane) settings, 1 bit per colour data overlay (superimpose) function and reduced frame-rate driving.

The multi-format driver 16 takes standard clock and control signals and a plurality of image data inputs, for example a colour grey-scale input and a binary colour input. The grey-scale input, D(1:n+m), is a parallel input of n+m bit width, where m corresponds to the number of most significant data bits of the grey-scale and n to the number of least significant data bits of the grey-scale. The input is represented as D(1:n+m) because it contains bits 1 to n+m. This input supplies grey-scale pixel image data with one of two resolutions: high resolution where all n+m bits are read by the driver 16, and low resolution where only the m MSBs are read by the driver 16. The binary input, D, is a 1-bit input which supplies independent black/white pixel image data.

The operation mode of the multi-format driver 16, i.e. the driver format, is controlled by the format control signals, also indicated in the diagram. In the example shown, three Bit-Resolution Control (BRC) control signals, SB, MB and NB are supplied, together with a Frame Rate Control (FRC) signal. The bit-resolution signals are distributed where necessary to the components of the multi-format driver 16 so that a particular driver format can be enabled with the lowest possible power consumption.

Figure 5 shows the trade off between the image quality and the power consumption, where it can be seen that the lowest power consumption is for one bit text data, and the highest power consumption is for n+m (e.g. 6 bit) video data with 1 bit overlay text.

The table in Figure 6 shows an example of how three bit-resolution signals SB, MB and NB, can be used to select the five possible driver format modes shown in Figure 5. Each

control signal is responsible for enabling specific circuits within the multi-format driver 16, as shown in Figure 7. SB enables the circuitry 18 associated with the single input data stream, D, which is used during the 1 bit display mode and when the overlay function is applied. MB enables the circuitry 20 associated with the most significant bits of the grey-scale input, D(n+1:n+m). NB enables the circuitry 22 associated with the least significant bits of the grey-scale input, D(1:n). In addition to the input signal combinations shown in the table, when all format control signals are 0, the multi-format driver 16 is essentially off.

The variable resolution Digital-to-Analogue-Converter (DAC) 24, shown in Figure 8, is used to convert the input data into analogue format suitable for driving the data lines of the panel. Parts of the circuit which are not used for a particular format, in particular the buffers during low-resolution mode, are disabled to reduce power consumption.

The frame rate control signal (FRC) can be used to enable circuitry for refreshing the active matrix display at slower update rates than the input frame rate. This can be particularly useful for saving power in situations where the input data is not changing, as for example in a static image.

According to the invention there is provided a driving arrangement and active matrix display as set out in the accompanying claims.

The invention thus allows the mode of operation of the display, and hence the power consumption and display quality, to be automatically controlled by the format of the input data itself. The operating mode and power consumption of the driver and display are optimised according to the data to be displayed. Therefore maximum battery life is obtained for portable equipment such as mobile communication terminals. The invention can be applied to a wide variety if integration technologies, such as Silicon IC display drivers or poly-Silicon monolithic drivers. The circuit overhead for the additional functionality is very modest, and hence there is a significant value-add for this type of display driver.

The invention can be implemented in the discreet controller IC, or else distributed within the driver ICs which can be connected to the active matrix by direct Chip On Glass (COG) bonding, or via flexible circuit connections. Alternatively, the circuits may even be integrated monolithically onto the same substrate as the active matrix devices, using Thin Film Transistor (TFT) technology such as high or low temperature poly-Silicon. The invention is particularly applicable to the control circuitry for mobile information displays, where power consumption is of prime importance.

Embodiments of the invention will now be described, by way of example only, with reference to the accompanying drawings, in which:

Figure 1 shows a typical active matrix display with analogue or digital drivers;

Figure 2 shows a typical active matrix display controller IC;

Figure 3 shows a conceptual application of multiple format image data;

Figure 4 shows a multi-format digital data driver;

Figure 5 power consumption versus image quality for a multi-format display;

Figure 6 shows a table of format control signals and selected display formats;

Figure 7 shows the power control of the data sampling circuits of a multi-format driver;

Figure 8 shows variable resolution digital to analogue conversion;

Figure 9 shows an embodiment of the invention, achieving content driven display format control.

Figure 10 shows the functional components of the data analysis means of Figure 9;

Figure 11 shows a generalised timing diagram for the data analysis means;

Figure 12 shows an embodiment of the data analysis means used to generate bit-resolution control signals.

Figure 13 shows a timing diagram for the bit-resolution control embodiment of Figure 12; and

Figure 14 shows an embodiment of the data analysis means used to detect a static image and to output a Frame Rate Control Signal.

A simplified block diagram of an embodiment of the invention is shown in Figure 9. A data analysis means 26 operates on input data, under the control of display timing signals in order to generate format control signals for a programmable multi-format digital data driver 28. The data analysis means 26 can be implemented remotely from the display driver 28, say within the LC controller (not shown), or it can be distributed within the data driver 28 itself.

Figure 10 shows a generalised view of the functional components within the data analysis means 26, which comprises two main functional units: a data analysis unit 30, and a format control register 32.

Within the data analysis unit 30 there exists an array of analysis logic blocks 34 which operate on the plurality of digital image data inputs during each frame of data. The logic blocks 34 can be simple combinational logic for detecting particular bit-sequences or bit-activities within the input data stream, or else they can be more complex functions such as adders or counters.

The outputs from the logic blocks 34 are latched in an array of temporary registers (represented by the SR block in Figure 10, and Figure 12 for example shows 3 such temporary registers), which are reset at the start of each frame of data, using for example the Vsync vertical synchronisation pulse. Each frame is made up of N lines,

and a vertical and horizontal synchronisation pulse occurs at the beginning of each frame and line respectively.

At the end of the frame of data the analysis results for that frame are clocked out of the temporary registers, using for example the gate pulse from the last row of the scan driver, and stored in the Format Control Register 32. The outputs of the format control register 32 are used as the format control signals for the next frame of data.

A generalised timing diagram for the data analysis means 26 is shown in Figure 11. At time T_0 the temporary storage registers 36 are 'reset' by the Vsync signal, which indicates the beginning of a new frame of data. The data enters the data analysis means 26 and is also input directly to the display driver 28, which is pre-configured according to the format control signals derived from the previous frame.

As each new line of data is clocked into the data analysis means 26, the array of logic blocks 34 monitor the data for particular activities or signature patterns, such as the number of bits, or the presence of text data etc. If a particular signature pattern is detected, the relevant logic block outputs a 'high' signal and the corresponding temporary storage registers 36 are 'set'. At time T_1, the high signal from the scan driver pulse of row N, G_N, indicates that the last row of data has been read into the data analysis means 26 and the results from the temporary storage registers 36 are clocked into the array of format control registers 32.

During the time between T_1 and T_2, the format control signals are used to re-configure the multi-format digital data driver 28 for the next frame of data, into the optimum or lowest power configuration for data of the same type as that received during the current frame.

Figure 12 shows an embodiment of the data analysis means 26 which is suitable for driving a multi-format digital data driver 28 with the format control signals shown in Figure 6. In this simple embodiment there are two logic blocks 38, 40, three temporary storage registers 42, 44, 46 and three format control signals (NB, MB, SB) to control the

bit resolution of the driver 28. During each frame of data, the 'OR' gates 38,40 detect the presence of activity within any of the MSB image data inputs, the LSB image data inputs or else the text data input. If any activity is detected, the corresponding 'SR latch' (42,44,46) is 'set' and the activity signals A_N, A_M and A_S are transferred to the format control register 32 at the end of the frame.

The timing diagram for this embodiment is shown in Figure 13, for various data formats. At time T_1, all activity signals are reset to 'low' by the frame synchronisation pulse VSync and the format control signals MB, NB and SB remain at the values determined by the previous frame, with MB 'high, and NB and SB 'low' i.e. the driver 28 is configured into m-bit mode. During the first frame of data, at time T_2, the MSB activity-signal A_M goes high immediately (as indicated by arrow 48), indicating that m-bit data is present. At time T_3, the data analysis means 26 detects activity in the LSB data as well as the MSB data, and so the activity-signal A_N goes high also (as indicated by arrow 50). At the end of the frame, all the activity signals are transferred into the format control register 32 at time T_4. Therefore, the driver 28 is configured into n+m bit mode at the beginning of the next frame also (as indicated by arrow 52). At time T_5 all the analysis signals are once again reset. At time T_6, the text analysis signal A_S also goes high (as indicated by arrow 54) so that for frame three the driver is configured into n+m bit mode, with 1-bit overlay also (as indicated by arrow 56), as illustrated in Figure 5.

Figure 14 shows an embodiment of the data analysis means 26 which is used to detect static image data and to output a format control signal which can be used by the multi-format driver 28 to disable the refresh of the liquid crystal, until such a time as is required by pixel leakage considerations. The basic operation of this embodiment is as follows.

At the heart of the analysis means 26 is a check-sum unit which is reset at the beginning of each frame of data and which performs a running addition of the input data within the frame. The output of the check-sum unit 58 is connected to a comparator 60 which compares the current check-sum with the check-sum from the previous frame. The

comparator 60 outputs a 'high' logic level if the check-sum for the current frame, n, is the same as the check-sum for the previous frame n-1.

At the end of the frame n, the output from the comparator 60 is transferred to the format control register 32, and the check sum for frame n is transferred into a latch 62, ready to be compared with the check sum for the next frame of data.

Although the described embodiment updates the display mode of the data driver after every frame, other intervals are possible. For example, the data driven display mode could be updated after each line of input data is analysed.

CLAIMS:

1. A driving arrangement for an active matrix liquid crystal display comprising:

(a) a multi-format digital data driver arranged to operate in a plurality of different display modes, to receive digital input data in a plurality of different formats, and to drive data lines of the liquid crystal display so as to cause an image to be displayed by the display corresponding to said input data; and

(b) data analysis means arranged to receive said digital input data, to determine the format of the input data, and to control the data driver to operate in the display mode corresponding to the format of the input data.

2. A driving arrangement as claimed in claim 1, wherein the data analysis means forms part of the data driver.

3. A driving arrangement as claimed in any preceding claim, wherein the data driver is arranged to consume less power in low resolution display modes compared to high resolution display modes.

4. A driving arrangement as claimed in any preceding claim, wherein said display modes include at least one 1-bit overlay mode.

5. A driving arrangement as claimed in any preceding claim, wherein the data analysis means analyses each frame of input data in turn, and updates the mode of the data driver at the end of each frame.

6. A driving arrangement as claimed in any preceding claim, wherein the data analysis means comprises frame comparison means for comparing each frame of input data with the next, and for determining if the input data for a number of consecutive frames is the same.

7. A driving arrangement as claimed in claim 6, wherein the data driver is arranged to operate at more than one refresh rate, and wherein the data analysis means is arranged to control the data driver to operate at a lower refresh rate if the comparison means determines that the input data has remained unchanged for a number of frames.

8. A driving arrangement as claimed in any preceding claim, wherein the data analysis means comprises a plurality of inputs each arranged to receive a single bit of said digital input data, and wherein at least some of said inputs are connected to a logic OR gate arranged to detect activity on one or more of said at least some inputs.

9. A driving arrangement as claimed in any preceding claim, wherein the data analysis means is arranged to supply format control signals to the data driver in order to control the display mode of the data driver.

10. A driving arrangement as claimed in claim 9, wherein said format control signals include at least high and low resolution control signals.

11. A driving arrangement as claimed in any preceding claim, wherein the data driver comprises a plurality of variable bit resolution digital to analogue converters.

12. A driving arrangement as claimed in any preceding claim, wherein the data driver comprises a plurality of digital data input channels arranged to receive said digital input data.

13. A driving arrangement as claimed in any preceding claim, wherein the data analysis means comprises a number of storage registers.

14. An active matrix liquid crystal display comprising a driving arrangement as claimed in any preceding claim.

15. An active matrix liquid crystal display as claimed in claim 14, wherein the driving arrangement is integrated monolithically onto the same substrate as the film transistors of the active matrix.

16. An active matrix liquid crystal display as claimed in claim 15, wherein said thin film transistors are poly-silicon

ABSTRACT

1. A driving arrangement for an active matrix liquid crystal display comprises:

(a) a multi-format digital data driver arranged to operate in a plurality of different display modes, to receive digital input data in a plurality of different formats, and to drive data lines of the liquid crystal display so as to cause an image to be displayed in the display corresponding to said input data; and

(b) data analysis means arranged to receive said digital input data, to determine the format of the input data, and to control the data driver to operate in the display mode corresponding to the format of the input data.

Figure 9

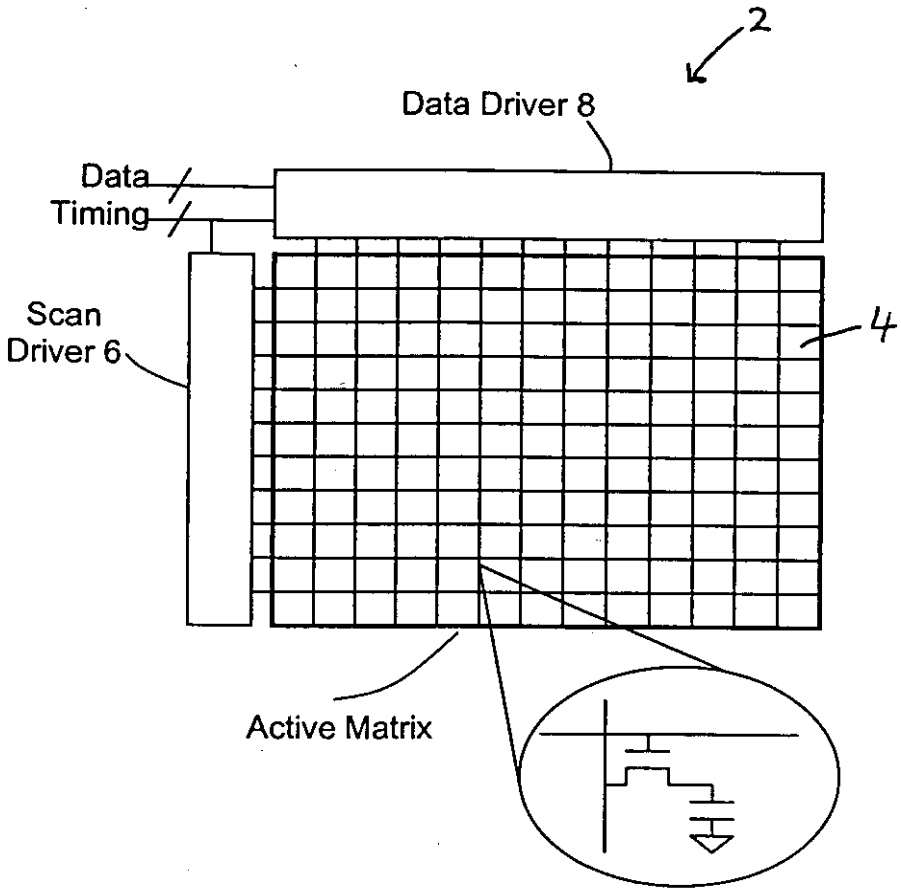

Figure 1: Prior art - Typical Active Matrix Display

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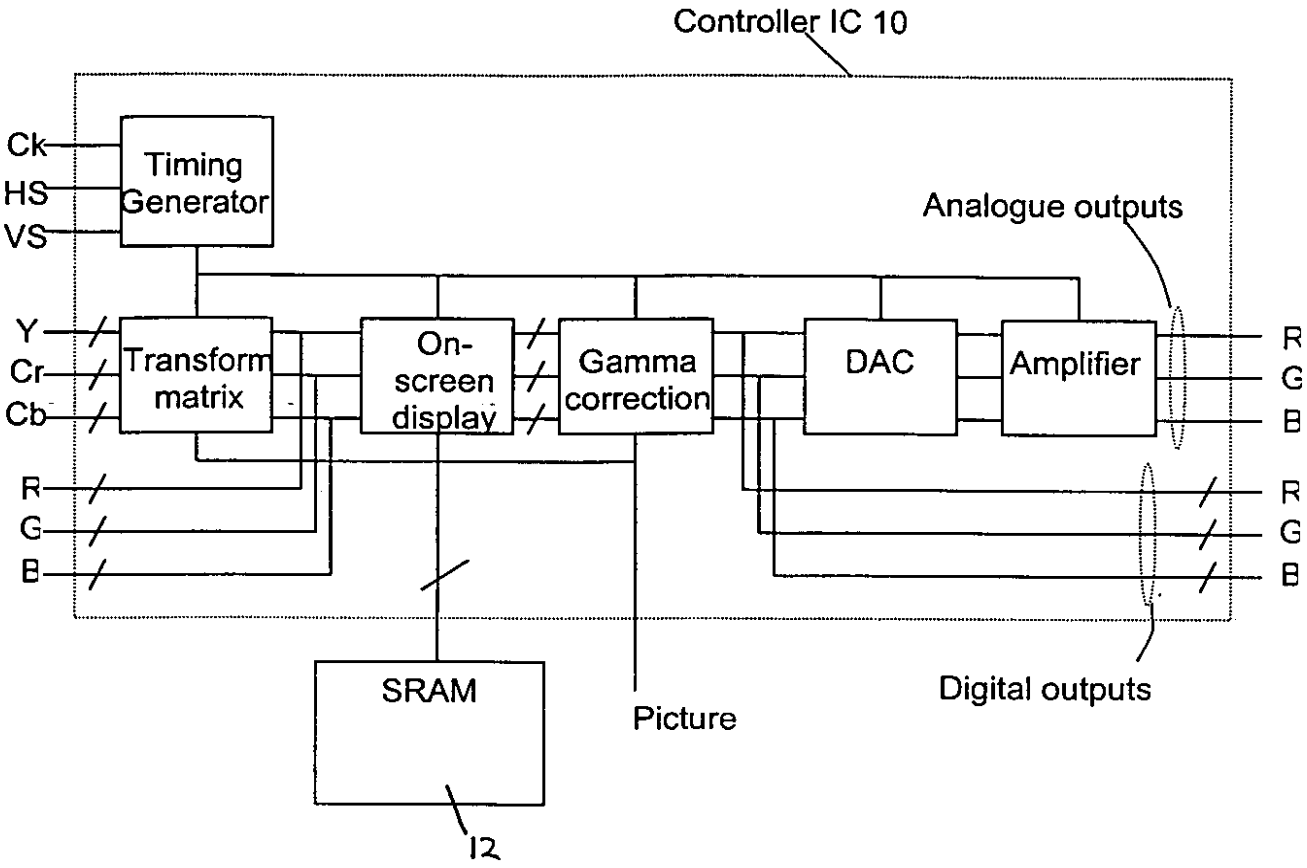

Figure 2 prior art - typical active matrix display controller IC

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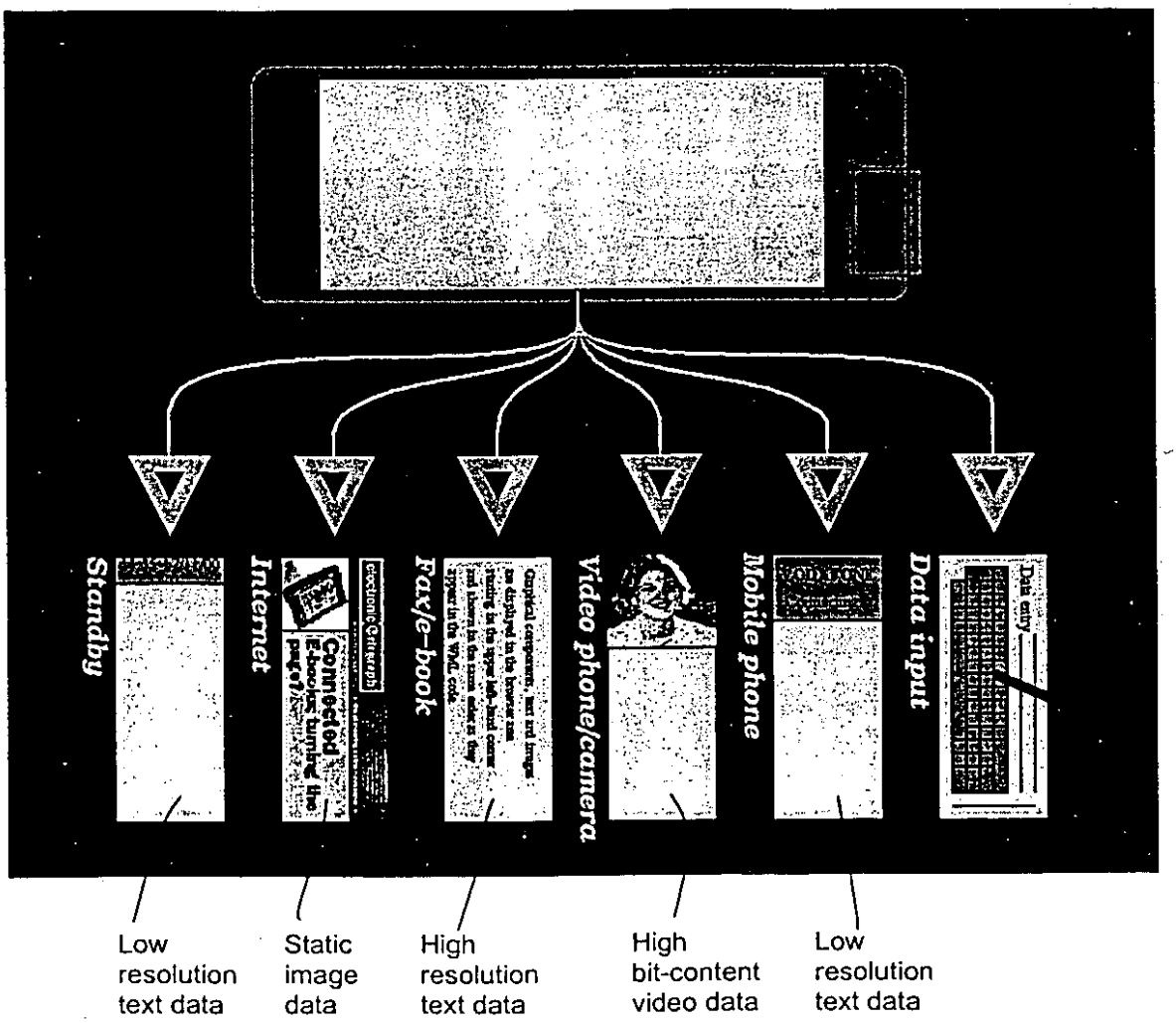

Figure 3: Conceptual application of multi-format image data

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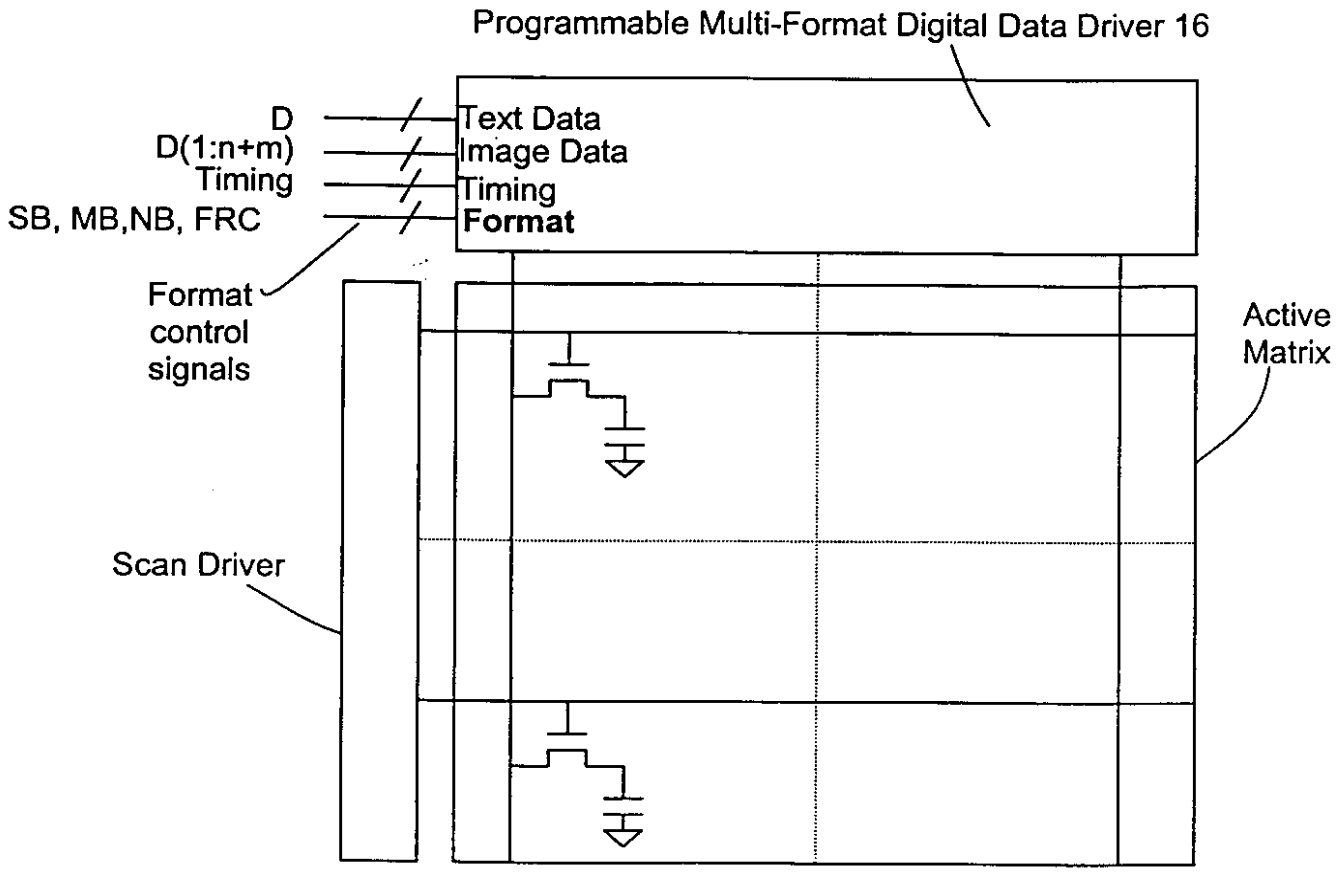

Figure 4: Multi-format digital data driver

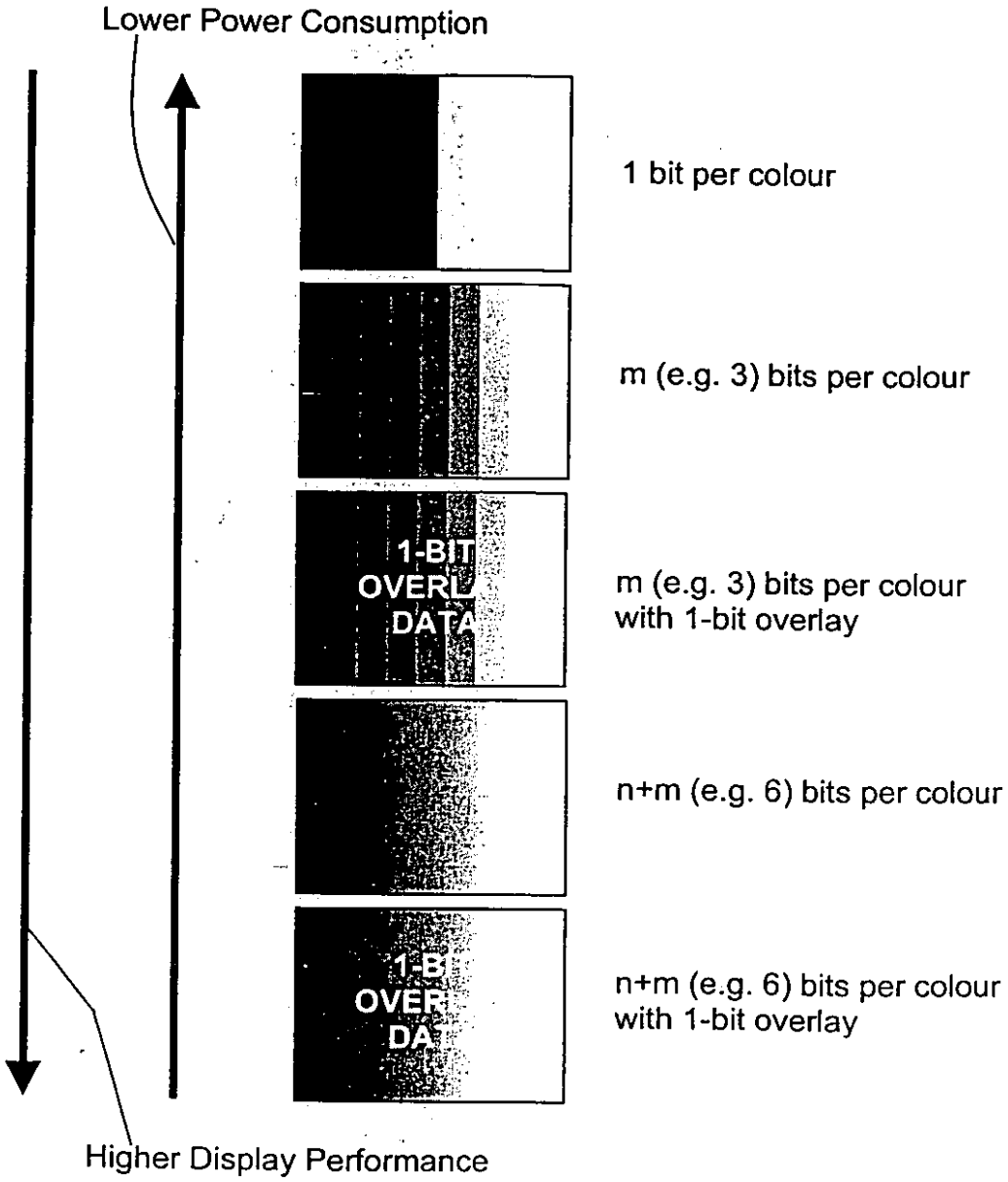

Figure 5: The trade-off between power consumption and image quality

Format Control			
NB	MB	SB	Driver Format
0	0	1	1-bit per colour
0	1	0	m bits per colour
1	1	0	n+m bits per colour
0	1	1	m bits per colour with 1-bit overlay
1	1	1	n+m bits per colour with 1-bit overlay

Figure 6: Table showing three Format Control Signals and selected format

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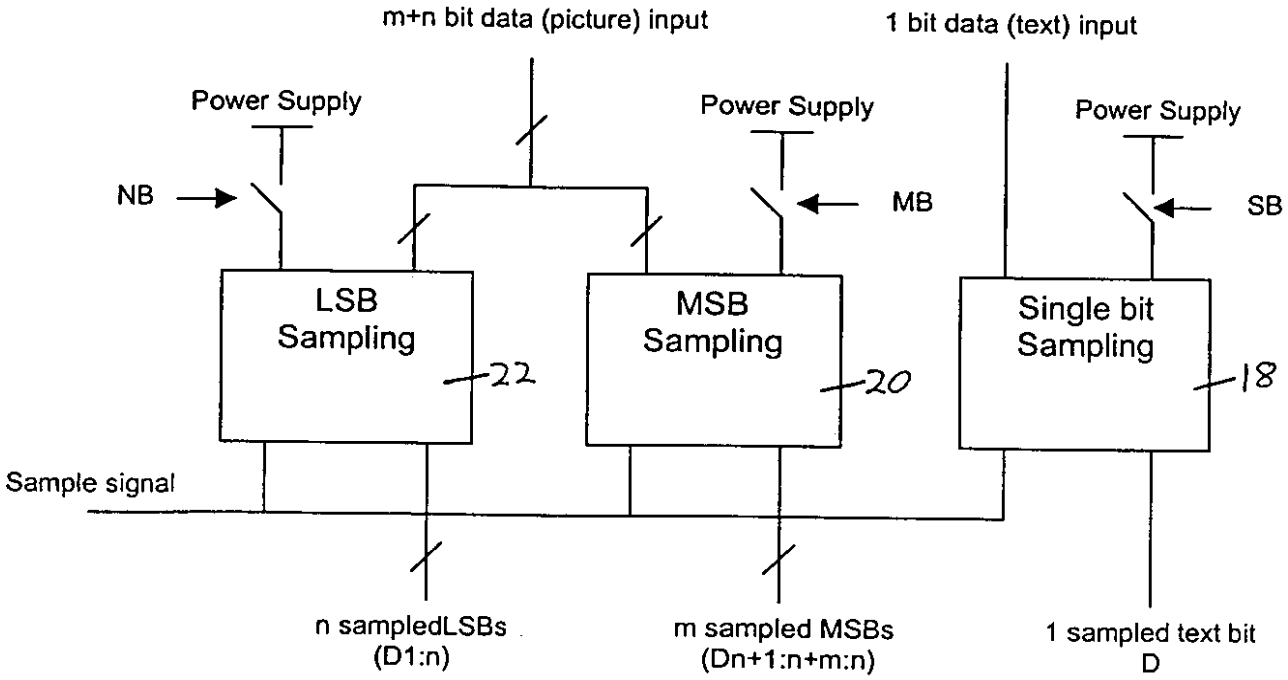

Figure 7: Power control within data sampling unit of multi-format driver

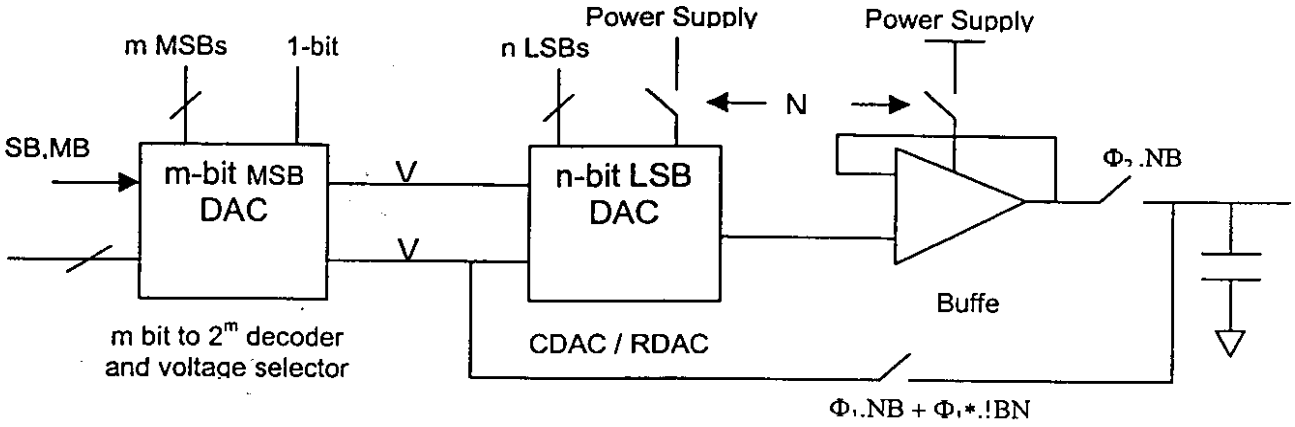

Figure 8 Variable resolution DAC with power control

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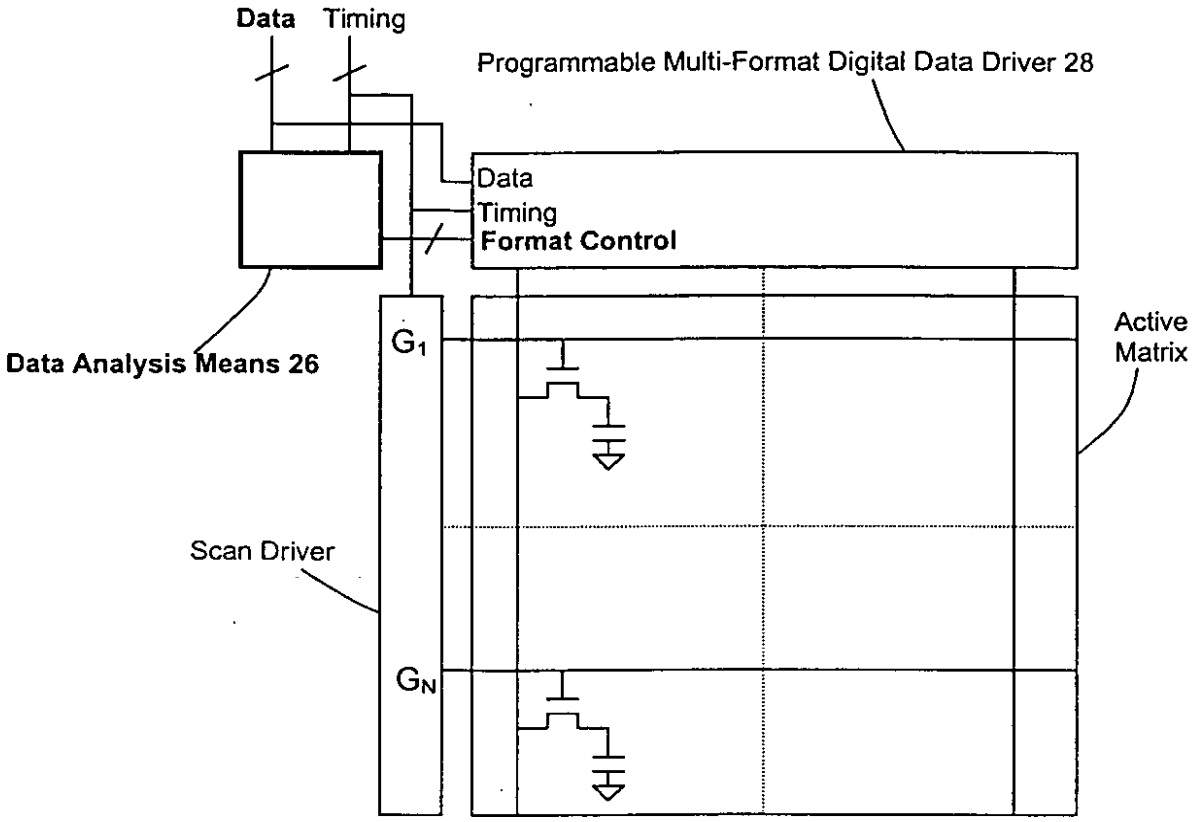

Figure 9 Basic embodiment of the invention – content driven format control

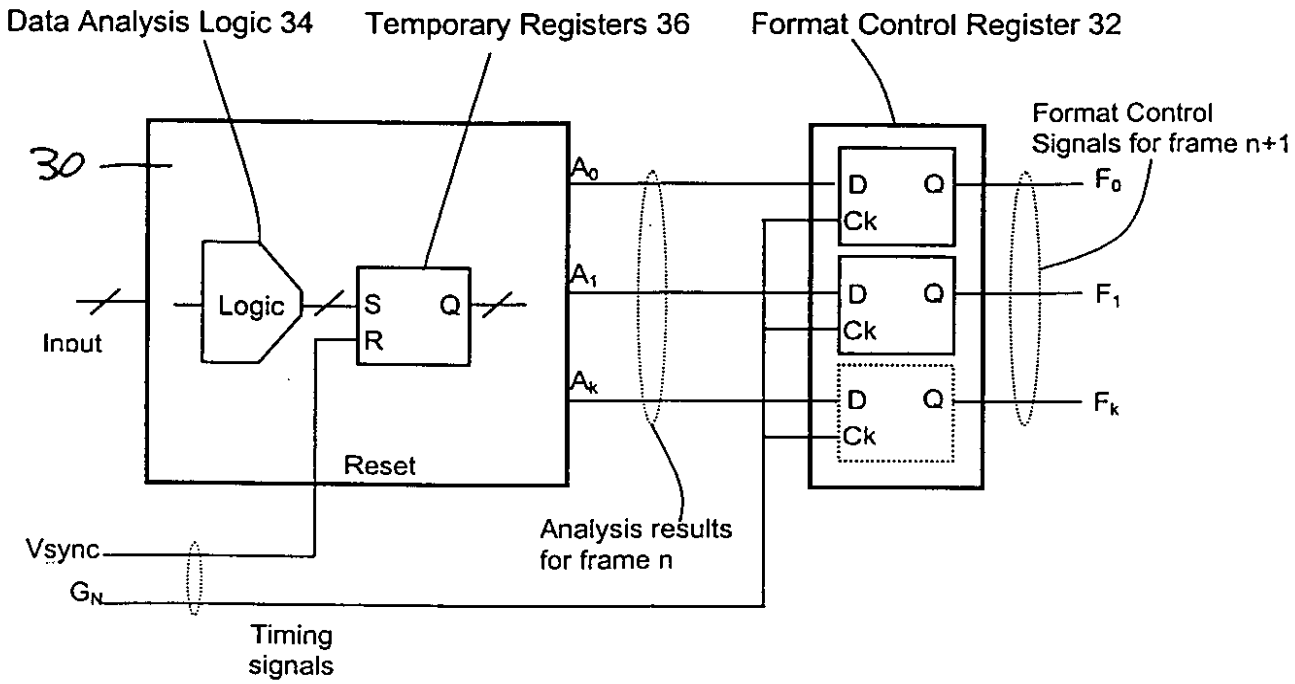

Figure 10 The functional blocks of the data analysis means

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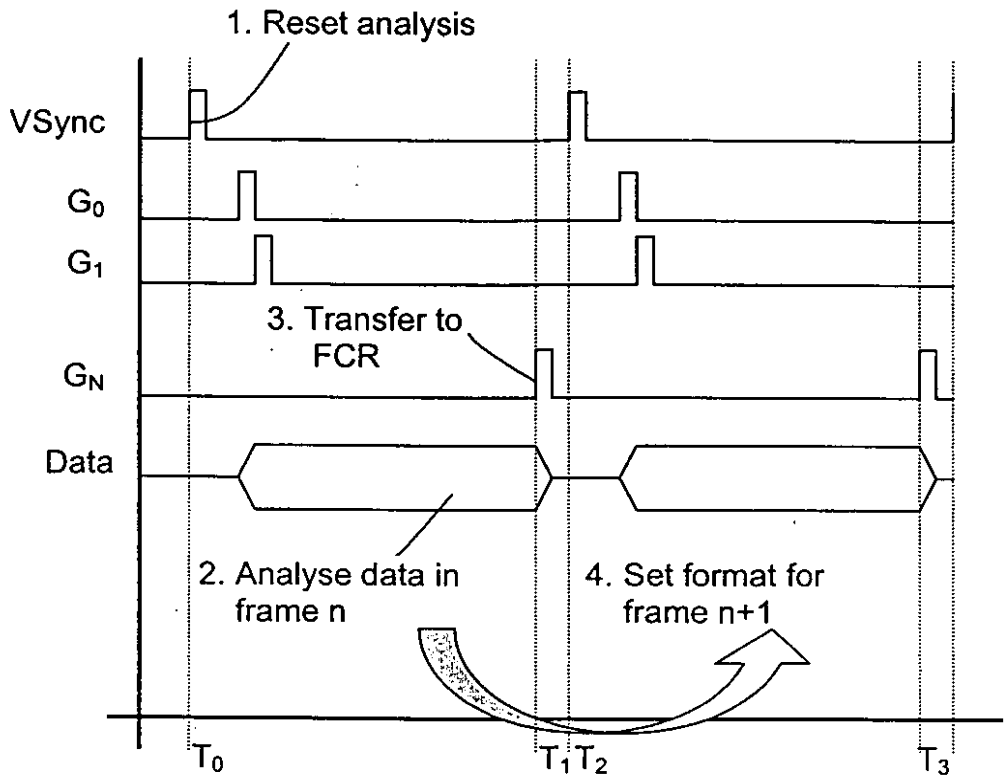

Figure 11 Generalised timing diagram for data analysis means

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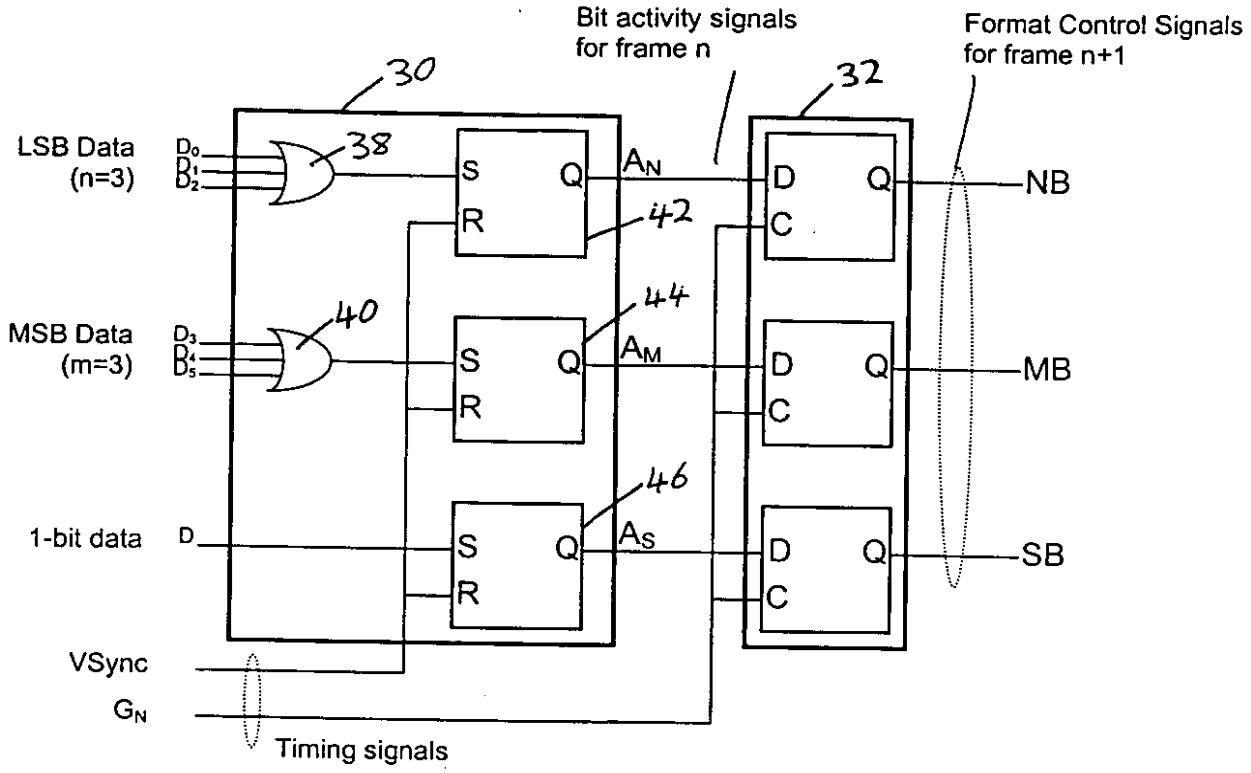

Figure 12 Embodiment of invention – generation of bit-resolution control signals

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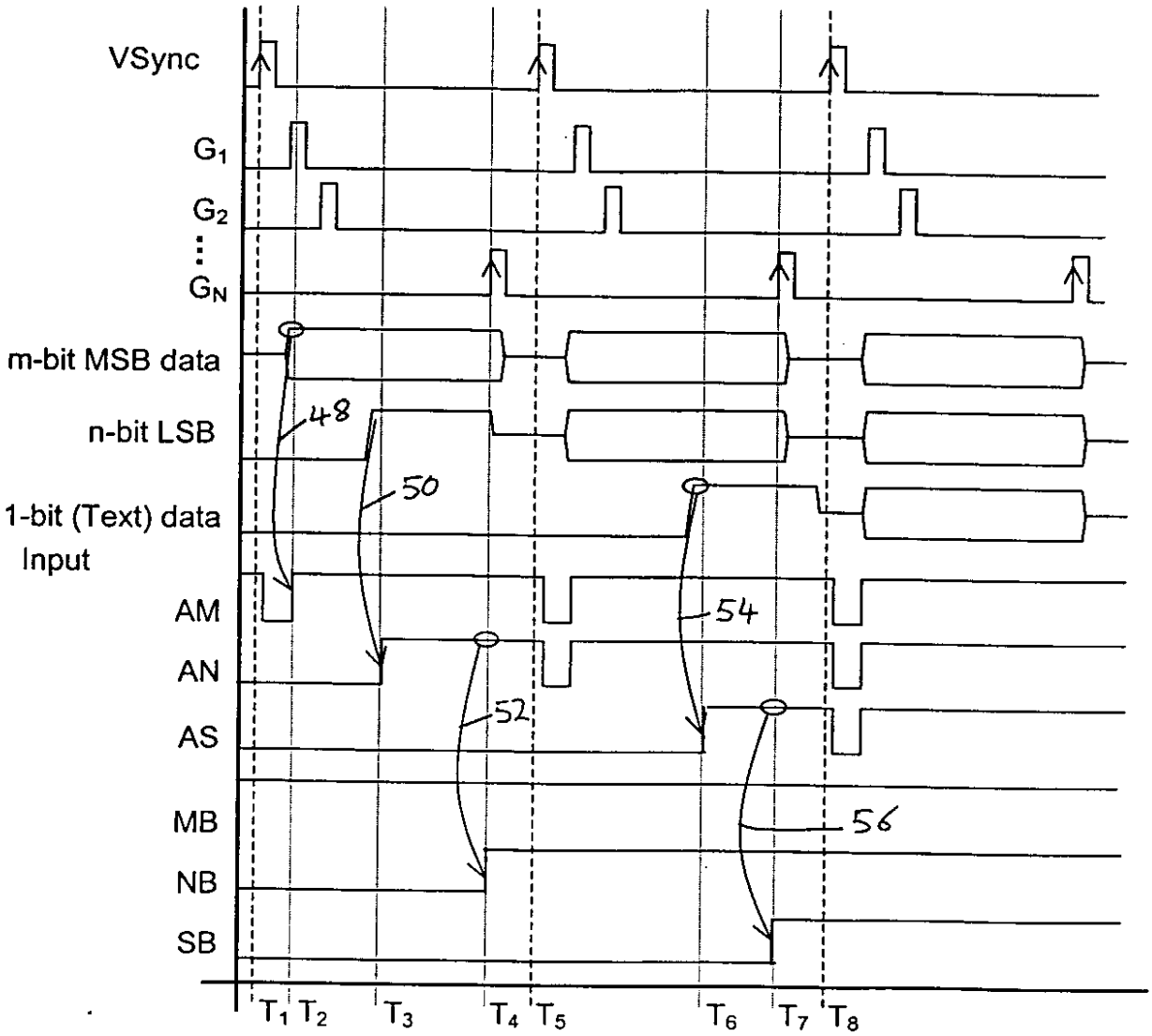

Figure 13: Timing diagram for bit-resolution embodiment

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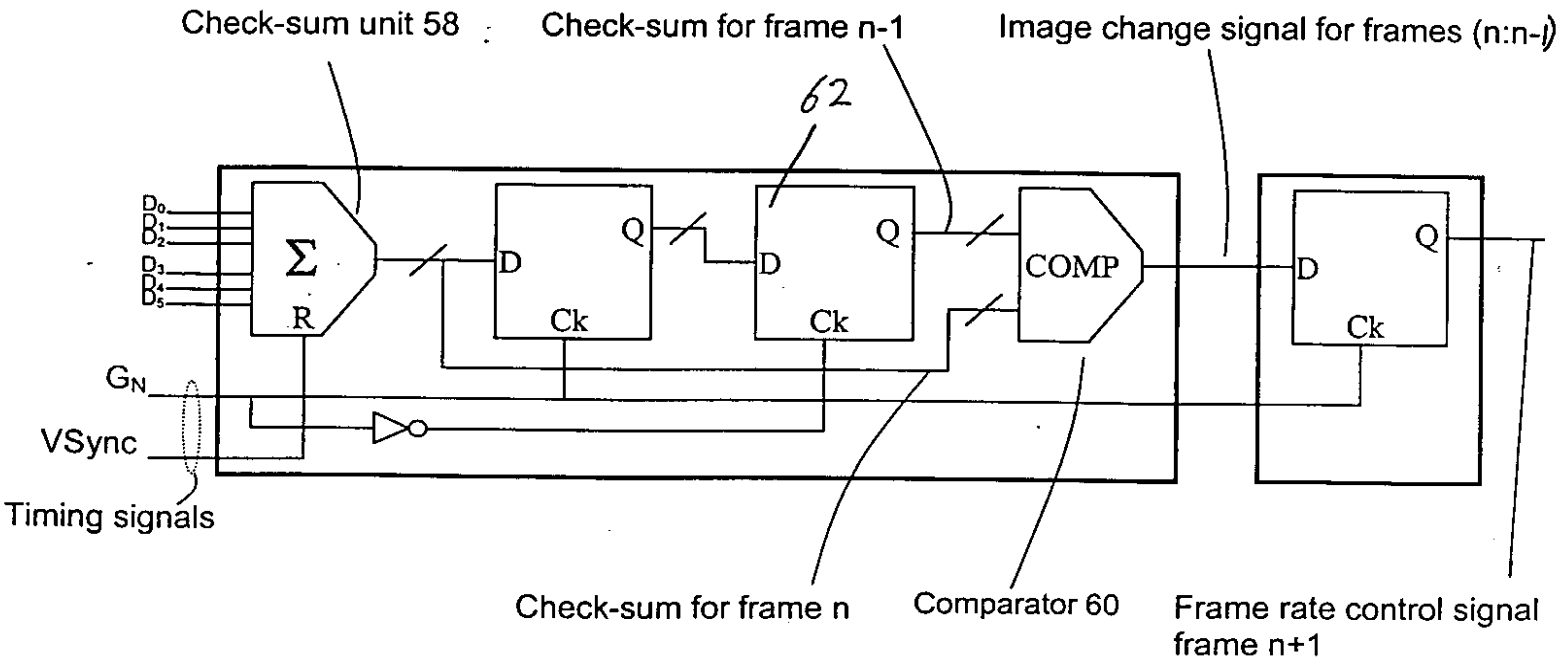

Figure 14: Embodiment of invention – analysis means for static image detection

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